

MOS FIELD EFFECT TRANSISTOR μ PA1913

PACKAGE DRAWING (Unit: mm)

P-CHANNEL MOS FIELD EFFECT TRANSISTOR FOR SWITCHING

 $0.32^{\,+0.1}_{\,-0.05}$

0.65-0.1

2.8 ±0.2 1.5

DESCRIPTION

The μ PA1913 is a switching device which can be driven directly by a 2.5-V power source.

The μ PA1913 features a low on-state resistance and excellent switching characteristics, and is suitable for applications such as power switch of portable machine and so on.

FEATURES

- Can be driven by a 2.5-V power source
- · Low on-state resistance

RDS(on)1 = 55 m Ω MAX. (VGS = -4.5 V, ID = -2.5 A)

RDS(on)2 = 58 m Ω MAX. (VGS = -4.0 V, ID = -2.5 A)

 $R_{DS(on)3} = 82 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = -2.7 \text{ V, ID} = -2.5\text{A})$

RDS(on)4 = 90 m Ω MAX. (VGS = -2.5 V, ID = -2.5A)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1913TE	6-pin Mini Mold (Thin Type)

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage	VDSS	-20	V
Gate to Source Voltage	Vgss	±12	V
Drain Current (DC)	ID(DC)	±4.5	Α
Drain Current (pulse) Note1	D(pulse)	±18	Α
Total Power Dissipation	P _{T1}	0.2	W
Total Power Dissipation Note2	P _{T2}	2	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C

1, 2, 5, 6 : Drain

0.95

0.95

1.9

2.9 ±0.2

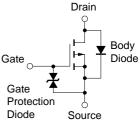
3 : Gate 4 : Source

EQUIVALENT CIRCUIT

0.9 to 1.1

 $0.16^{+0.1}_{-0.06}$

0 to 0.1



Marking: TE

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1 %

2. Mounted on FR4 board, $t \le 5$ sec.

Remark

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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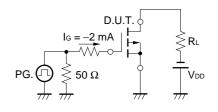
ELECTRICAL CHARACTERISTICS (TA = 25 °C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	Ipss	Vps = -20 V, Vgs = 0 V			-10	μΑ
Gate Leakage Current	lgss	Vgs = ±12 V, Vps = 0 V			±10	μΑ
Gate Cut-off Voltage	V _{GS(off)}	$V_{DS} = -10 \text{ V}, I_{D} = -1 \text{ mA}$	-0.5	-1.1	-1.5	V
Forward Transfer Admittance	y fs	$V_{DS} = -10 \text{ V}, I_{D} = -2.5 \text{ A}$	3	8.8		S
Drain to Source On-state Resistance	RDS(on)1	Vgs = -4.5 V, ID = -2.5 A		44	55	mΩ
	RDS(on)2	Vgs = -4.0 V, ID = -2.5 A		46	58	mΩ
	RDS(on)3	Vgs = -2.7 V, ID = -2.5 A		60	82	mΩ
	RDS(on)4	Vgs = -2.5 V, ID = -2.5 A		66	90	mΩ
Input Capacitance	Ciss	V _{DS} = -10 V		700		pF
Output Capacitance	Coss	V _G S = 0 V		208		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		100		pF
Turn-on Delay Time	td(on)	V _{DD} = -10 V		300		ns
Rise Time	t r	I _D = -2.5 A		528		ns
Turn-off Delay Time	td(off)	$V_{GS(on)} = -4.0 \text{ V}$		242		ns
Fall Time	tr	$R_G = 10 \Omega$		698		ns
Total Gate Charge	Q _G	V _{DD} = -16 V		6.0		nC
Gate to Source Charge	Qgs	I _D = -4.5 A		2.1		nC
Gate to Drain Charge	Q _{GD}	Vgs = -4.0 V		2.8		nC
Diode Forward Voltage	V _{F(S-D)}	IF = 4.5 A, VGS = 0 V		0.86		V
Reverse Recovery Time	trr	IF = 4.5 A, VGS = 0 V		32		ns
Reverse Recovery Charge	Qrr	$di/dt = 10 A/\mu s$		2.2		nC

TEST CIRCUIT 1 SWITCHING TIME

D.U.T. \bigcirc RG \bigcirc RG \bigcirc VGS (-) \bigcirc VGS (-) \bigcirc VGS (-) \bigcirc VGS (-) \bigcirc 10 % \bigcirc VGS (-) \bigcirc 10 % \bigcirc VGS (-) \bigcirc 10 % \bigcirc 10 %

TEST CIRCUIT 2 GATE CHARGE



90 %

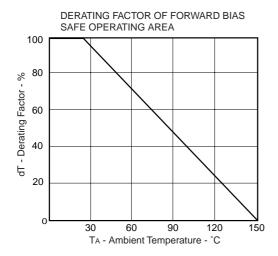
90 %

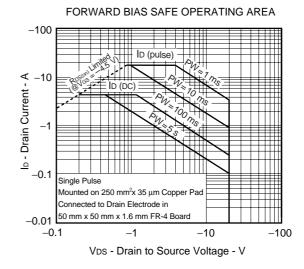
-10 <u>%</u>

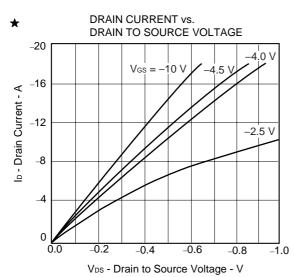
VGS(on)

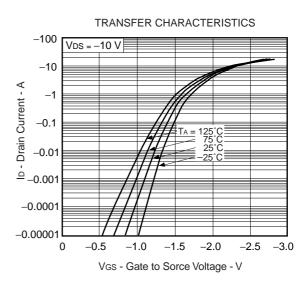


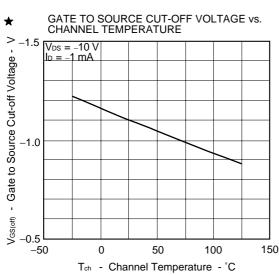
TYPICAL CHARACTERISTICS (TA = 25°C)

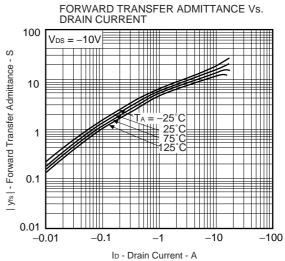




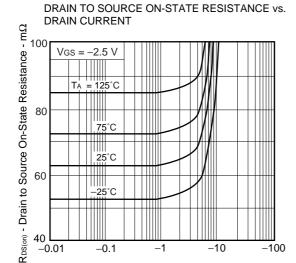


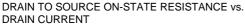




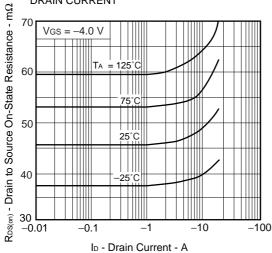


3

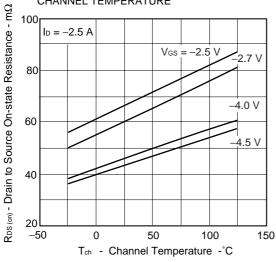




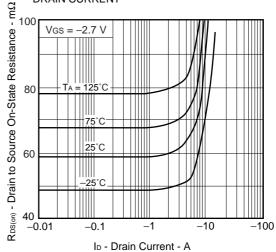
ID - Drain Current - A



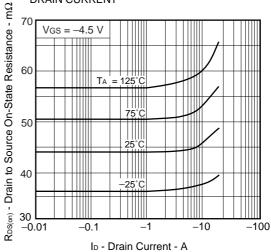
DRAIN TO SOURCE ON STATE RESISTANCE vs. CHANNEL TEMPERATURE



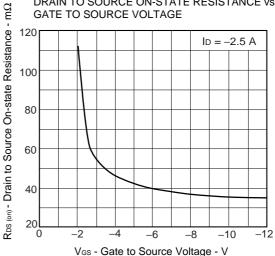
DRAIN TO SOURCE ON-STATE RESISTANCE vs. **DRAIN CURRENT**

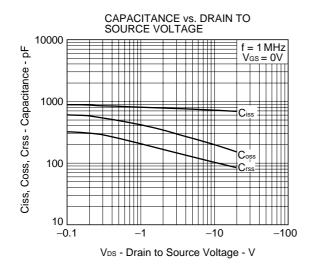


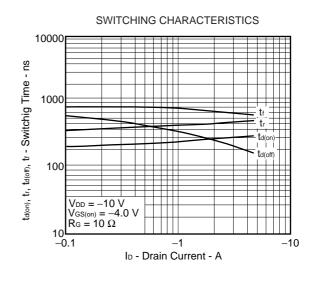
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



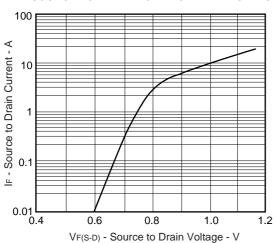
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

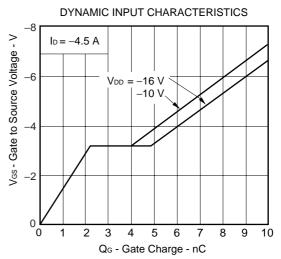




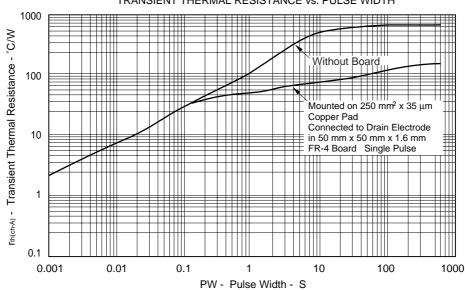








TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



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NEC

 μ PA1913

[MEMO]

NEC μ PA1913

[MEMO]

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